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**--- Abstract ---**

Title: Scalable integration of superconducting qubits with three-dimensional wiring

Superconducting quantum circuits are one the most promising platforms to realize a large-scale quantum computer.
Although more than 100-qubit quantum processors are becoming available, the scalability of wiring and packaging is still one of the biggest challenges to be overcome.
As quantum error correcting codes require at least a two-dimensional array of qubits, wring from the third dimension is essential to scale up the size of superconducting circuits.
To this end, a variety of wiring methods have been proposed such as flip-chip bonding [1], through-silicon via (TSV) interposers [2], and spring-loaded pogo pins [3,4].

In this work, we present a scalable integration of a large-scale superconducting qubit chip based on a tileable circuit design and three-dimensional wiring of coaxial cables. Our superconducting qubit chip has a 4-qubit unit-cell circuit that can be repeatedly used to increase the number of qubits on a chip. The control and readout coaxial lines are connected perpendicular to the chip from the backside. The microwave transmission from the coaxial cables to the qubits is realized reliably by using spring-loaded pogo pins and TSVs structures on the chip. This fully vertical wiring makes it possible to scale up the number of qubits by just tiling the same circuit pattern in a lateral direction. We implemented a 64-qubit superconducting chip based on the tileable circuit design. Compared with conventional wiring such as on-chip airbridges or wire bonding, our fully three-dimensional wiring can have low control signal crosstalk. The low-crosstalk tileable superconducting qubit integration relaxes the difficulty of calibrating microwave-driven qubit gates as well as extending the number of qubits on a chip.

References:

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